

IC-e6-cPCIb 6U/cPCI PICMG 2.16 PowerPC SBC

IC-e6-cPCIb is a cPCI processor board based on the Freescale e600 processors MPC7447A or MPC7448. It is designed to provide the highest level of performance and integration available today.

The MPC7448 is a high-performance embedded e600 core. These low power PowerPC processors are ideal for application in the fields of defense, industrial automation and medical imaging.

IC-e6-cPCIb can be used in many highly integrated applications like :

- Leading-edge computing.
- Embedded network control.
- Signal processing, etc.



Description

IC-e6-cPCIb is powered by one or two MPC7448 (optionally MPC7447A), being part of the PowerPC processor family. This processor features a high-frequency superscalar PowerPC core capable of issuing four instructions per clock cycle into 11 independent execution units : four integer units, one double-precision floating point unit, four AltiVec units, load/store and branch processing units. The MPC7448 provides 3900 DMIPS @ 1,7GHz. Owing to the Dynamic Frequency Switching, the core frequency can be changed "on the fly" to reduce the power consumption.

The dual processor version runs with SMP Linux (Symmetrical multi Processor).

IC-e6-cPCIb runs as a host system controller or a peripheral board with an automatic slot detection. The PCI interface runs up to 66MHz in PCI mode and up to 133MHz in PCI-X mode. A second PCI/PCI-X bridge controls two PMC mezzanine cards.

IC-e6-cPCIb implements a DiscoveryTMIII chipset to fill out the processor. This solution includes major enhancements such as : data streaming on MPX bus, read memory latency and cache coherency improvements. The MV64460 indeed, adds 2 Mbits of high speed burst SRAM, two XOR DMA (useful for RAID, iSCSI) and four IDMA engines.

IC-e6-cPCIb integrates many communication functions : three Giga Ethernet channels, one console port. An USB2 controller provides three high/full speed ports. A quad UART provides four additional asynchronous channels.

Thanks to its optional SATA controller, **IC-e6-cPCIb** can directly manage several storage devices.

IC-e6-cPCIb can be used with many major RTOS and Linux.

Main features

Processor Unit

- ▶ MPC7448 running at 1.4 or 1.7 GHz with :
 - L1 caches : 32KB Inst. and 32KB Data with parity.
 - 1MB of L2 integrated cache with ECC.
- ▶ 512MB, 1 or 2GB of SDRAM-DDR with ECC.
- ▶ 64, 128 or 256MB of soldered Mirror Flash.
- ▶ Up to 1 GB soldered Nand Flash.
- ▶ 256KB (128-bit wide access) of high speed SRAM.
- ▶ 128KB or 1MB BSRAM (non-volatile memory).
- ▶ PPC Real Time clock and four 32 bit-timers.
- ▶ Calendar clock with supercap backup.
- ▶ Temperature sensor and monitoring.

The MPC7447A version only runs at 1 GHz.

I/O subsystem

- ▶ 32 or 64-bit CompactPCI bus interface.
- ▶ Two PMC sites with IO routing toward J3 / J5.
- ▶ Marvell DiscoveryTM III system controller :
 - Three Ethernet 10/100/1000TX ports with :
 - Support for Jumbo frames.
 - Virtual Cable Tester on line.
 - Two routed on rear J3 and one on the front panel.
 - One serial interface for the front console port.
- ▶ One USB2 controller with two rear and one front ports.
- ▶ GPIO on J3/5
- ▶ A four channels SATA controller with two ports on J3 and two ports available through an on-board planar connector.

Accessories

- ▶ Engineering kit for debug : JTAG/COP, console cable, etc.
- ▶ 6U Rear Transition Module (RTM) providing : 2 Giga RJ45, USB2, four RS232/422 ports, two SATA connectors and an HD68 connector for the PMC IO.

IC-e6-cPCIb is available in standard, extended, rugged grades.

IC-e6-cPC1b

PICMG 2.16 PowerPC Single Board Computer

On-board firmware

Our basic firmware takes in charge Freescale's new MPC7448 or the MPC7447A and the Marvell chipset Discovery III initialization. This on-board firmware, based on the open-source UBOOT, is an efficient set of software stored in a secured flash.

UBoot

It is called by the reset vector when the board is powered up. It initializes the PowerPC and the DiscoveryTMIII system controller, performs a comprehensive Power-on self-tests (PBIT), before jumping into different applications according to the values stored in memory. If the board acts as a Monarch PMC, the software executes an enumeration step, otherwise it waits for the PCI startup sequence from the host. In standalone mode the board directly runs the configured application.

The firmware allows loading files from Ethernet via Bootp, running files in RAM or flashing them. In addition, it allows some monitor functions such as : display or modify the RAM data. To end with, it enables the user to perform maintenance tests.

IC_Bios

This module allows the user to access the specific IC-e6-cPC1b hardware resources via an easy-to-use API. This module is used as a library with Vxworks and as a dynamically loaded library module for Linux.

IC-BSP basic

These BSPs products are based on the standard distribution of the OS editor. They take in charge hardware initialization, interrupt handling and generation, hardware clock and timer services, memory management, PCI management, mapping of memory spaces, serial ports, MAC driver for Gigabit ports.

Interface Concept provides BSP for VxWorks® and Linux® operating systems. Other RTOS (LynxOS, Integrity...) can be ported on request.. The dual processor model runs LINUX SMP.

Interface features

cPCI bus interface

Auto-detect System or Peripheral slot
PCI or PCI-X 32/64-bit

PMC slots

Signaling : 3.3 and 5V tolerant
PCI , PCI-X 32/64-bit at 33, 66 or 100 MHz
Address/Data : A32/D32
PMC IO routed on J3/J5
IEEE 1386 compliant

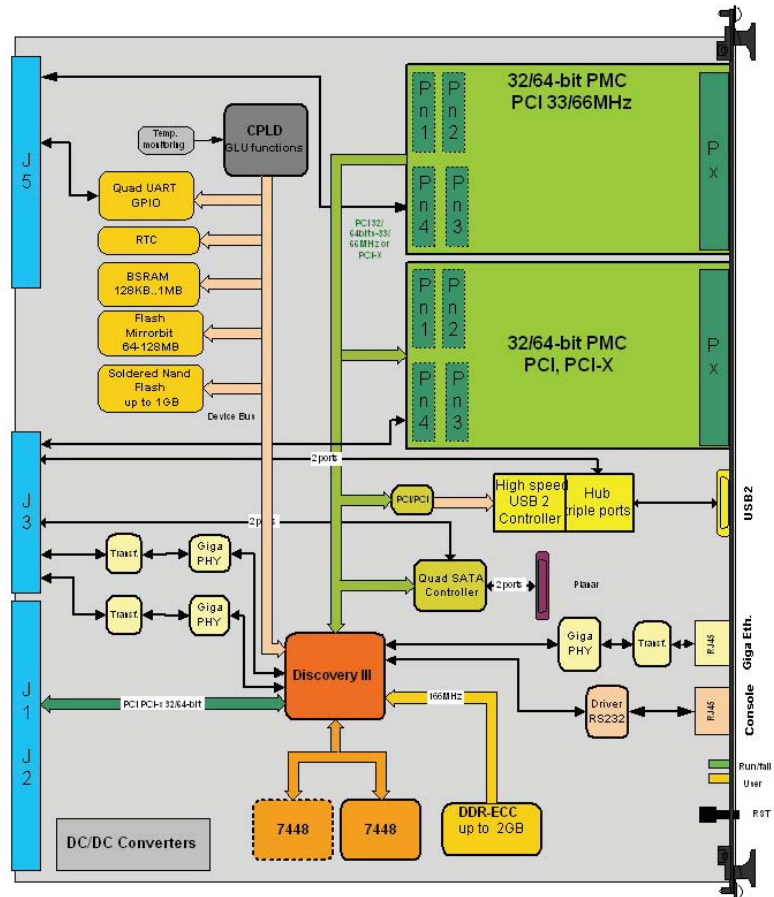
J3 connector

2 Giga Ethernet Compliant with PIGMG2.16
Two USB2
Two SATA ports
GPIO

Front connectors

One 10/100/1000BT
One USB2 (High/full speed)
One console port

Block Diagram



Environnement Specifications:

Please refer to information below.

Ordering Information:

Please consult the **IC-e6-cPC1b datasheet** at www.interfaceconcept.com (listing all products reference and environment grades availability).

This document supersedes any earlier documentation relating to the products referred to herein. The information contained in this document is current at the date of publication. It may subsequently be updated or withdrawn without notice.

