

## Dual-CPU 64-bit Power™ Platform Processor

### The PWRficient Advantage

- Two 64-bit power-efficient superscalar out-of-order CPUs offer high-end processing capabilities at modest power dissipation.
- Two integrated memory controllers provide low-latency access to DDR2-1066 memory banks.
- An integrated 2MB L2 cache provides substantial on-chip storage for code and data.
- A configurable, coherent I/O subsystem provides a choice of high-speed serial I/Os, including PCI Express, 10GbE, and 1GbE.
- A sophisticated demand-balancing DMA controller and associated offload engines provide efficient data movement and processing, including encryption, checksum computations, and streaming XOR generation.



The PWRficient PA6T-1682M high-performance platform processor—which combines two 2GHz PA6T CPUs, two DDR2 memory controllers, 2MB of L2 cache, and a flexible I/O subsystem—is a versatile building block for high-performance computing and embedded applications.

PWRficient provides industry-leading performance per watt for multigigahertz computational applications and multigigabit throughput applications. PWRficient achieves this breakthrough with a ground-up design that optimizes power dissipation in all aspects of its novel system architecture, which comprises an entire platform on a chip.

The CONEXIUM™ coherent crossbar is an on-chip fabric that interconnects the two 64-bit superscalar CPUs, two DDR2 memory controllers, a dual-ported 2MB L2 cache, and the ENVOI™ I/O subsystem to deliver on-chip symmetric multiprocessing with coherent I/O.

Dynamic power management on the PWRficient 1682M results in a worst-case total power dissipation of only 25W with both CPUs running at 2GHz and memory and I/O interfaces active at their maximum rate. Typical power dissipation ranges from 5W in portable applications to 13W in high-performance applications that require 10 Gigabit Ethernet interfacing; in power-saving modes, power dissipation drops to around 1W (typical).

The ENVOI I/O subsystem provides 24 configurable SERDES lanes for high-speed serial I/O, which may be used for PCI Express, XAUI, or SGMII interfacing in a wide range of configurations.

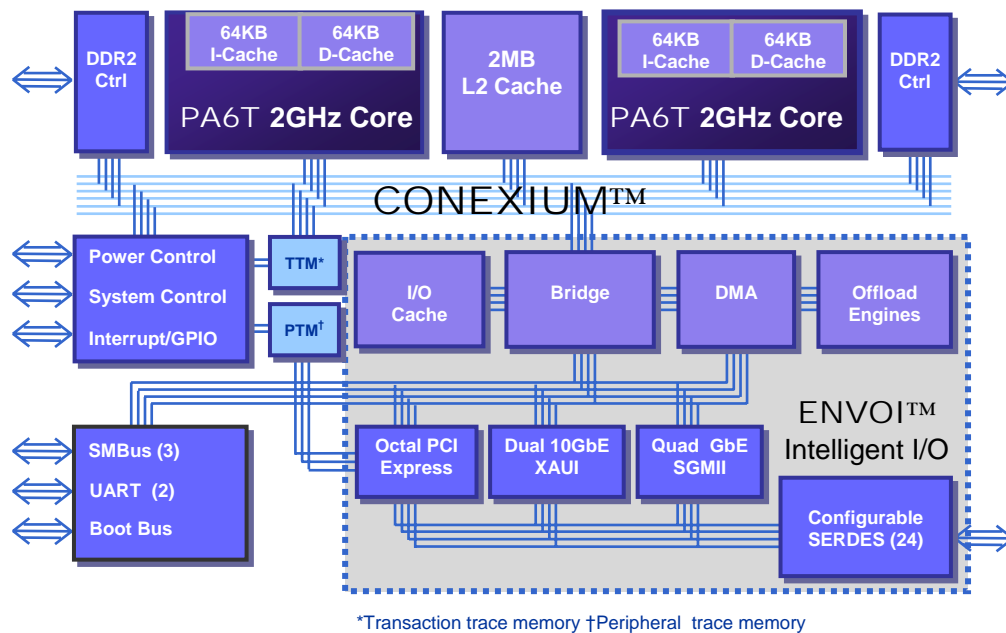
There are 8 PCI Express engines, supporting link widths of 1, 2, 4, 8, and 16 lanes for general peripheral connection with up to 4GB/s bandwidth per engine. The two XAUI (10 Gigabit Ethernet) and four SGMII (10/100/1000Mbit Ethernet) protocol engines each feature packet processing, including line-rate packet filtering, VLAN flow control, and TCP/IP acceleration. The two XAUI links can be optionally used as SGMII links, enabling a total of 6 SGMII links.

ENVOI includes a multichannel DMA engine to perform block copies from memory to memory, memory to device, or device to device. Optionally, computation and transformation functions may be applied to the data as it is copied; these offload functions include bulk encryption and the computation of hash, CRC, and XOR values. ENVOI includes a coherent I/O cache and adaptive prefetch unit to improve system performance.

The system controller includes power and CPU-frequency management circuits, watchdog and regular timers, an interrupt controller compatible with the OpenPIC standard, two UARTs, three SMBus channels, and a debug controller. The local/boot bus supports LPC and SPI NAND Flash, CompactFlash™ (including TrueIDE mode) and general multiplexed address/data protocols.

PWRficient provides server-class reliability. All internal SRAMs that hold modified data are protected with single-bit correct, double-bit detect ECC, and CONEXIUM transactions are parity protected. The memory controller supports a combined ECC/CRC to correct single-bit errors and detect double-bit errors and single chip failures.

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### Two 64-bit Power PA6T CPUs

- Power Architecture version 2.0.4 compliant

### Superscalar CPU with Out-of-Order Issue

- Quad fetch, triple issue per cycle
- 64-instruction-deep schedule buffer
- In-order retirement to allow precise exceptions
- Strong store ordering to simplify programming
- Fast branch predictor and 16K-entry branch-history table

### Fully Pipelined Execution Units

- Single load/store execution unit
- Dual integer execution units
- Full floating-point unit
- Full VMX unit

### 64KB Instruction Cache, 64KB Data Cache, Accelerated MMU Operation

- 1024-entry 4-way hardware-managed TLB
- Hardware page table walker with prefetch
- Support for multiple page sizes (4KB–1GB)

### Bus Interface for Compute and I/O-intensive Tasks

- Up to 16 cache misses may be outstanding
- 6 merge buffers for uncached stores
- Option for up to 15 outstanding uncached loads
- 12-channel hardware prefetch engine

### Virtualization Support

- Supports multiple, different operating systems simultaneously on each CPU
- Supports industry-standard hypervisors

### 24 Lanes of SERDES Shared Among

- 8 PCI Express links
  - Can have one 16x lane link
  - Other links are 8x, 4x, 2x, or 1x
- 2 XAUI links (each requires 4 lanes)
- 4 SGMII links (each requires 1 lane)
- The 2 XAUI links can also be used as SGMII links (total of 6)

### 2MB 8-way Associative Shared L2 Cache

- Flexible way allocation, locking

### DMA Engine with Cryptography, RAID, and TCP Offload

- AES, DES, 3DES, ARC4, Kasumi
- SHA-1, SHA-256, MD-5, Generic CRC
- IPSEC and SSL

### Two DDR2-1066 Memory Controllers (8 Ranks per Controller)

- Supports standard 1-, 2-, and 4-rank 64/72-bit DIMMs
- Up to 16GB per channel (using 2Gb-density DRAMs)
- 266–533MHz clock (533–1,066MHz data rate)

### System Support

- Interrupt controller, UARTs, SMBus
- Local bus supports LPC, SPI Flash, CompactFlash, IDE
- JTAG debug interface

### Physical Parameters

- 35mm organic PBGA, 1156 balls on 1mm pitch
- 25W worst-case power dissipation at 2GHz
- Operating junction temp 0–100°C
- RoHS compliant; Pb free
- 65nm CMOS technology

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